AMENDMENTS TO THE CLAIMS:

Complete Listing of Claims

1. (currently amended) A switched variable capacitor, comprising:

a switching field-effect transistor, having first and second source/drain regions, and having a gate for receiving a control signal;

a first capacitor, connected between a first terminal and the first source/drain region of the switching transistor;

a second capacitor, connected between a second terminal and the second source/drain region of the switching transistor; and

first and second ~~complementary~~ bias transistors, having a conduction path connected between a bias voltage and the first and second source/drain regions of the switching transistor, respectively, and having a gate coupled to the gate of the switching transistor, so that the first and second complementary bias transistors are turned on when the switching transistor is turned off.

2. (currently amended) The capacitor of claim 1, wherein the switching transistor is of a first conductivity type;

and wherein the first and second ~~complementary~~ bias transistors are of a second conductivity type.

3. (currently amended) The capacitor of claim 1, further comprising:

third ~~first~~ and fourth ~~second~~ bias transistors, having a conduction path connected between a reference voltage and the first and second source/drain regions of the switching transistor, respectively, each having a gate coupled to the gate of the switching transistor, so that the third ~~first~~ and fourth ~~second~~ bias transistors are turned on when the switching transistor is turned on.

4. (currently amended) The capacitor of claim 3, wherein the gates of the first and second ~~complementary~~ bias transistors are coupled to the gate of the switching transistor so that the first and second ~~complementary~~ bias transistors are turned off when the switching transistor and the third ~~first~~ and fourth ~~second~~ bias transistors are turned on.

5. (currently amended) The capacitor of claim 3, wherein the channel width/length ratio of the switching transistor is substantially larger than the channel width/length ratios of the first and second ~~complementary~~ bias transistors and the third ~~first~~ and fourth ~~second~~ bias transistors.

6. (currently amended) The capacitor of claim 1, wherein the bias voltage is selected to have a polarity and magnitude that strongly reverse-biases the source/drain regions ~~junctions~~ of the switching transistor with respect to an underlying substrate or well, as the case may be.

7. (original) The capacitor of claim 1, wherein the first and second capacitors are metal-to-metal capacitors in an integrated circuit.

8. (currently amended) An array of switched variable capacitors, comprising:

a plurality of capacitances, binary-weighted from a smallest capacitance to a largest capacitance, each of the plurality of capacitances connected between first and second terminals and having a control signal, each of the plurality of capacitances including at least one switched variable capacitor that comprises:

a switching field-effect transistor, having first and second source/drain regions, and having a gate for receiving a control signal;

a first capacitor, connected between a first terminal and the first source/drain region of the switching transistor;

a second capacitor, connected between a second terminal and the second source/drain region of the switching transistor; and

first and second ~~complementary~~ bias transistors, having a conduction path connected between a bias voltage and the first and second source/drain regions of the switching transistor, respectively, and having a gate coupled to the gate of the switching transistor, so that the first and second ~~complementary~~ bias transistors are turned on when the switching transistor is turned off; and

a plurality of control lines, binary-weighted to represent a digital control word, each control line associated with a corresponding one of the plurality of capacitances.

9. (original) The array of claim 8, wherein each of the first and second capacitors are of the same capacitance;

wherein a least significant capacitance, corresponding to the smallest capacitance, includes a single switched variable capacitor controlled by the least significant control line;

wherein the next least significant capacitance, corresponding to the next smallest capacitance, includes a pair of switched variable capacitors connected in parallel between the first and second terminals, and controlled by the next least significant control line;

and wherein more significant capacitances each include a plurality of switched variable capacitors, of a number corresponding to the binary-weighting of its associated control line.

10. (currently amended) The array of claim 8, wherein each switching transistor is of a first conductivity type;

and wherein each of the first and second ~~complementary~~ bias transistors is of a second conductivity type.

11. (currently amended) The array of claim 1, wherein each of the switched variable capacitors further comprises:

third ~~first~~ and fourth ~~second~~ bias transistors, having a conduction path connected between a reference voltage and the first and second source/drain regions of the switching transistor, respectively, each having a gate coupled to the gate of the switching transistor, so that the third ~~first~~ and fourth ~~second~~ bias transistors are turned on when the switching transistor is turned on;

wherein the gates of the first and second ~~complementary~~ bias transistors are coupled to the gate of the switching transistor so that the first and second ~~complementary~~ bias transistors are turned off when the switching transistor and the first and second bias transistors are turned on.

12. (currently amended) The array of claim 11, wherein the channel width/length ratio of each switching transistor is substantially larger than the channel width/length ratios of the first and second ~~complementary~~ bias transistors and the third ~~first~~ and fourth ~~second~~ bias transistors in its switched variable capacitor.

13. (currently amended) The array of claim 8, wherein the bias voltage is selected to have a polarity and magnitude that strongly reverse-biases the source/drain junctions ~~junctions~~ of the switching transistor with respect to an underlying substrate or well, as the case may be.

14. (original) The array of claim 8, wherein each of the first and second capacitors are metal-to-metal capacitors in an integrated circuit.

15. (currently amended) A method of digitally controlling a switched variable capacitor, comprising the steps of:

in a maximum capacitance state, turning on a switching transistor connected in series with first and second capacitors between first and second terminals, the first and second capacitors connected to first and second source/drain regions of the switching transistor, respectively; and

in a minimum capacitance state:

turning off the switching transistor; and

turning on first and second ~~complementary~~ bias transistors connected between the first and second source/drain regions of the switching transistor, respectively, and a bias voltage, the bias voltage selected to strongly reverse bias regions ~~junctions~~ of the first and second source/drain regions of the switching transistor with respect to an underlying substrate or well, as the case may be.

16. (currently amended) The method of claim 15, further comprising, in the maximum capacitance state:

turning on third and fourth bias transistors connected between the first and second source/drain regions of the switching transistor, respectively, and a reference voltage.